

PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Mark WALLIS

Serial No. (unknown)

Filed herewith

APPARATUS AND METHOD FOR  
CONTROLLING VOLTAGE  
REGULATOR AND POWER  
SUPPLY APPARATUS



**CLAIM FOR FOREIGN PRIORITY UNDER 35 U.S.C. 119**  
**AND SUBMISSION OF PRIORITY DOCUMENT**

Assistant Commissioner for Patents

Washington, D.C. 20231

Sir:

Attached hereto is a certified copy of applicant's corresponding patent application filed in United Kingdom on 22 November 2000, under No. 0028488.5.

Applicant herewith claims the benefit of the priority filing date of the above-identified application for the above-entitled U.S. application under the provisions of 35 U.S.C. 119.

Respectfully submitted,  
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November 20, 2001

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23NOV00 2585865-17 001631  
P01/7700 0.00-0028488.5

2. Patent application number

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0028488.5

22 NOV 2000

3. Full name, address and postcode of the or of each applicant (underline all surnames)

NEC Technologies (UK) Limited  
The Imperium (Level 3)  
Imperial Way  
Reading  
Berkshire RG2 0TD

Patents ADP number (if you know it)

If the applicant is a corporate body, give the country/state of incorporation

United Kingdom

7012313002

4. Title of the invention

Method for Improving the Efficiency of Linear Regulators

5. Full name, address and postcode in the United Kingdom to which all correspondence relating to this form and translation should be sent

Reddie & Grose  
16 Theobalds Road  
LONDON  
WC1X 8PL

Patents ADP number (if you know it)

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6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and (if you know it) the or each application number

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Claim(s)	2
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Statement of inventorship and right to grant of a patent (*Patents Form 7/77*)

Request for preliminary examination and search (*Patents Form 9/77*) 1

Request for substantive examination (*Patents Form 10/77*)

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11. I/We request the grant of a patent on the basis of this application.

Signature

Date

22 November 2000

*A J Robson*

12. Name and daytime telephone number of person to contact in the United Kingdom

A J ROBSON  
020-7242 0901

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LINEAR REGULATORS

This invention relates to linear voltage regulators.

Linear voltage regulators are well known electronic devices. They are used to produce a steady output voltage at a predetermined level from an input voltage which may vary. The input voltage is higher than the output voltage and heat is dissipated in the regulator. The power dissipated given a constant load current is proportional to the voltage drop between the input and the output. For example, in a battery operated system where the operating voltage of the circuitry is significantly lower than the battery voltage, reducing the power dissipation in the regulator will lead to improved battery life. It will also reduce the thermal efficiency requirements of the regulator thereby allowing a small and cheaper package and pass transistor to be used.

Traditionally, power supply efficiency has been improved by replacing the pass transistor with a switched inductor. A buck converter uses such an arrangement. However, the inductor tends to be a large and expensive component and is generally not suitable for miniaturisation.

Preferred embodiments of the present invention provide a method and circuitry for improving the efficiency of a linear regulator without using ferro-electric components. In particular, preferred embodiments of the invention reduce the input voltage to the linear regulator by switching small amounts of charge between capacitors.

The invention is defined with more precision in the appended claims to which reference should now be made.

A preferred embodiment of the invention will now be described in detail by way of example with reference to the accompanying drawings in which:

**Figure 1** is a block diagram of a system embodying the invention;

**Figure 2** shows the capacitor voltages for various states of the circuit of **Figure 1**;

5       **Figure 3** shows an implementation of a second embodiment of the control circuitry of **Figure 1**; and

**Figure 4** shows the voltage signal transitions for various points in the circuit of **Figure 3**.

10       A preferred embodiment of the invention is shown in **Figure 1**. This comprises a DC power supply or battery 2 which supplies an input voltage  $V_{in}$ . This is connected in parallel with two capacitors  $C_1$  and  $C_2$ .  $C_1$  is separated from  $V_{in}$  by a switch  $S_1$ . A further switch  $S_2$  separates capacitors  $C_1$  and  $C_2$ . A linear regulator 4 is connected  
15 across the circuit downstream of capacitor  $C_2$  and has an output which produces a voltage  $V_{out}$  and a current  $I_{load}$ .

A control circuit 6 monitors the input voltage to the linear regulator 4 and in response to this supplies control signals to switches  $S_1$  and  $S_2$  which can be closed.  
20  $S_1$  when closed will enable a capacitor  $C_1$  to charge.  $S_2$  when closed will allow capacitor  $C_2$  to charge from capacitor  $C_1$  at the same time as providing input charge to the linear regulator 4.

25       The control circuit is responsive to the voltage of the input to the linear regulator. When this voltage falls below a predetermined level, equal to the minimum required to maintain the output voltage  $V_{out}$ , the control circuit opens switch  $S_2$  and closes switch  $S_1$ , in that order. This causes  $C_1$  to be charged up to the battery  
30 voltage, whereupon switch  $S_1$  is reopened and  $S_2$  is closed (again in that order). A charge is transferred from the battery to  $C_1$  in the first stage where switch  $S_1$  is closed and in the second phase when  $S_1$  is open and  $S_2$  is closed, charge is transferred from  $C_1$  to  $C_2$  until the voltages  
35 across the capacitors are equalised. Subsequently, if a



constant load current  $I_{load}$  is drawn from the regulator, the voltage on the capacitors will decrease linearly until the switching threshold is reached again. Typically, the switching threshold will be set to such a level that recharging the capacitor  $C_1$  by closing switch  $S_1$  and opening switch  $S_2$  and switching back to discharge of capacitor  $C_1$  by opening switch  $S_1$  and closing switch  $S_2$  can happen before the input voltage to the linear regulator falls beneath the minimum required to maintain voltage  $V_{out}$ .

The traces in Figure 2 show the voltages across the capacitors linked to the switching cycle, assuming that there are no resistive losses in the circuit. In practice, there will of course be resistive losses and the traces will be modified accordingly.

The average voltage at the input to the regulator is the average of  $V_{C2}$ , and is given by:

$$V_{ave} = \frac{V_{set} + V_{out} + V_{do}}{2}$$

$V_{set}$  is determined by considering the energy transferred between the capacitors. The energy stored in  $C_1$  while  $S_1$  is closed is given by:

$$E_1 = \frac{C_1 \cdot V_{in}^2}{2}$$

The energy remaining in  $C_2$  at the moment  $S_2$  closes is given by:

$$E_2 = \frac{C_2 \cdot (V_{out} + V_{do})^2}{2}$$

By conservation of energy, the combined energy of  $C_1$  and  $C_2$  in parallel is given by:

$$E_c = E_1 + E_2 = \frac{C_1 \cdot V_{in}^2}{2} + \frac{C_2 \cdot (V_{out} + V_{do})^2}{2}$$

Also:

$$E_c = \frac{(C_1 + C_2) \cdot V_{set}^2}{2}$$

Therefore:  $V_{set} = \sqrt{\frac{2 \cdot E_c}{C_1 + C_2}} = \sqrt{\frac{C_1 \cdot V_{in}^2 + C_2 \cdot (V_{out} + V_{do})^2}{C_1 + C_2}}$

From the above equations, it can be deduced that the  
5 power drawn from the battery is given by:

$$P = I_{load} \cdot V_{ave} = \frac{I_{load}}{2} \cdot \left[ \sqrt{\frac{C_1 \cdot V_{in}^2 + C_2 \cdot (V_{out} + V_{do})^2}{C_1 + C_2}} + V_{out} + V_{do} \right]$$

The power drawn from the battery without the  
switch/capacitor circuit is given by:

$$P_{old} = I_{load} \cdot V_{in}$$

10 Therefore the improvement in power efficiency given  
by the circuit (ignoring power lost during switching due  
to gate capacitance and switch/capacitor series  
resistance) is:

$$\frac{P}{P_{old}} = \frac{1}{2 \cdot V_{in}} \cdot \left[ \sqrt{\frac{C_1 \cdot V_{in}^2 + C_2 \cdot (V_{out} + V_{do})^2}{C_1 + C_2}} + V_{out} + V_{do} \right]$$

15 It can be seen by examination of Eq.1 that the best  
efficiency is obtained when  $C_2 \gg C_1$  such that

$V_{set} \Rightarrow (V_{out} + V_{do})$ . Then the improvement in efficiency  
approaches the ratio:

$$\frac{P}{P_{old}} = \frac{V_{out} + V_{do}}{V_{in}}$$

The period T between successive activations of the switches is dependent on the load current:

$$T = \frac{[V_{set} - (V_{out} + V_{do})] \cdot (C_1 + C_2)}{I_{load}}$$

5 or substituting for  $V_{set}$ :

$$T = \frac{(C_1 + C_2)}{I_{load}} \left[ \sqrt{\frac{C_1 \cdot V_{in}^2 + C_2 (V_{out} + V_{do})^2}{C_1 + C_2}} - (V_{out} + V_{do}) \right]$$

10 So the switching period is inversely proportional to the load current, as would be expected. The period can be increased (to save power lost in switching) by making  $C_1$  as large as possible.

The circuit of Figure 3 is a more detailed implementation of an embodiment of the invention. The portion of the circuit corresponding to the control circuit 6 of Figure 1 is shown in dotted outline.

15 Switches  $S_1$  and  $S_2$  are P-channel FET devices. The feedback arrangement of the voltage which in Figure 1 is from the input voltage to the linear regulator (given by the voltage on capacitor  $C_2$ ) is in this implementation replaced by feedback from the voltage on capacitor  $C_1$  and

20 from the voltage output of the regulator for  $V_{out}$ .  $V_{out}$  is the voltage input to a voltage divider  $R_1$  and  $R_2$  and the output of this divider is provided to one input of a comparator 8. The voltage on capacitor  $C_1$  is fed by a further voltage divider  $R_3$  and  $R_4$  to the other inverted

25 input of comparator 8.

The output of comparator 8 is provided to the two inputs of a flip-flop comprising a pair of NAND gates and a pair of AND gates. The output of the comparator goes directly to the input of a first NAND gate 10 and by the inverter 12 to the second NAND gate 14. The output of NAND gate 14 is connected to the other input of NAND gate 10 and, the output of NAND gate 10 is connected to the second input of NAND gate 14. The output of NAND gate 10 is also connected to an input of an AND gate 16 whilst the output of NAND gate 14 is connected to an input of an AND gate 18. The other input of each of these AND gates 16 and 18 is connected to a start/enable line. The purpose of the AND gates is to enable the regulator to start up and Figure 4 shows the voltage at various points in the circuit during start up and subsequent operation following the application of a signal to the start/enable line.

When the start/enable signal is low (probably by default when battery power is applied), both FET switches  $S_1$  and  $S_2$  are forced on, and the battery voltage is applied directly to the regulator input. This enables the regulator to start up as normal in low efficiency mode. This mode may also be used if the battery voltage falls to the point where it ceases to provide any efficiency improvement or, alternatively, may be used in situations where harmonic interference caused by switching is undesirable (e.g., in a radio subsystem).

When the start/enable signal is set high, e.g., by a micro-controller I/O port, the voltage on  $C_1$  will be higher than the output of the regulator and the output of comparator 8 will be low. Therefore,  $V_{gs1}$  (the  $S_1$  enabling voltage) will be high and so  $S_1$  will be open, and  $V_{gs2}$  ( $S_2$  enabling voltage) will be low, which means  $S_2$  will be closed. If a load current is drawn from the regulator, the voltage on the capacitors will fall. When  $V_{C1}$  reaches a predetermined switching point,  $V_{threshold}$ , the comparator output will go high. The switching point is set relative

to the output voltage of the regulator,  $V_{out}$ , and can be adjusted by varying the ratio  $R_3$  to  $R_4$ . It should be chosen such that the voltage across the regulator remains larger than the maximum dropout voltage  $V_{do}$  (the voltage drop across the regulator) at all times and under all load current conditions. Clearly, allowance needs to be made for the time taken to recharge  $C_1$ , considering that in a practical implementation there will be a finite switching time for the FET's, and series resistance means that the capacitors do not charge instantaneously.

When the comparator output switches to high in response to a reduction in  $V_{out}$ , the flip-flop will cause  $V_{gs2}$  to go high thereby opening  $S_2$  and will cause  $V_{gs1}$  to go low, thereby closing  $S_1$ .  $C_1$  will then charge and  $V_{C1}$  will increase. This will cause the comparator output to go low when it reaches a predetermined level, thereby causing  $S_1$  to open again and  $S_2$  to close and the cycle to begin again.

The small amount of resistance in the switching circuit which was mentioned above consists of the series resistance of the battery, or voltage source, the series resistance of the switches and interconnections, and the series resistance of the capacitors. The effect of this is twofold. Firstly, it will reduce the efficiency of the circuit due to energy dissipation. Secondly, it will introduce a delay of the transfer of charge between the battery and capacitors. Any inductance in the circuit will also add to this delay. This means that the "on" time of  $S_1$  must be increased to allow  $C_1$  to be fully charged.

The circuit shown in Figure 3 relies on propagation delays through the feedback circuitry to provide this delay. A more deterministic method might include a hysteresis component in the comparator, such that the voltage on  $C_1$  has to approach the battery voltage before the comparator switches back.

A second consideration is the time required to turn the transistors on and off. This is determined by the size of the transistor, the gate capacitance, and the drive capability of the AND gates. Clearly, if there is a period during which both transistors are switched on,  $C_2$  will be directly charged from the battery, and the voltage of the regulator input will be consequently higher. This leads to a reduction in efficiency of the circuit which can be dramatic. The NAND/inverter circuit is used to prevent any overlap between switching off one transistor and switching on the other. Nevertheless, this relies on the propagation delay through the NAND gates being greater than the switching time of the transistors. The delay can be increased by inserting extra delay buffers in the feedback path between the output of one NAND gate and the input of the other.

Another effect of transistor switching time is increased loss whilst the transistors are partially on and, hence resistive. Ideally, very fast transistors should be used. However, this can usually only be achieved at the expense of series resistance and/or maximum current capability. Therefore, a compromise must be made based on the load requirements. Furthermore, it should be noted that the peak current flow from the battery  $I_{peak}$  can be high if  $S_1$  switches very quickly. A slower turn on time may be desirable to limit the transient current and possible associated noise problems.

The most obvious practical consideration is in the selection of the capacitors. Clearly, low ESR dielectrics such as ceramics will contribute less to the overall loss in the switching system. However, the larger the value of  $C_1$ , the lower the switching frequency, (furthermore,  $C_2$  should be significantly larger than  $C_1$ ) and this will increase efficiency. This is because a significant amount of power is lost in the switching of the gates and the transistors and therefore a low switching frequency is

desirable. Preferably, therefore,  $C_2$  should be chosen to be as large as possible within the space and cost limitations of the system.

5       The switching transistors and the feedback circuit  
could be integrated into a BiCMOS process with the linear  
regulator Bipolar/CMOS (CMOS = Complementary Metal Oxide  
Semiconductor). This would mean that the only external  
components required would be the capacitors. All linear  
10       regulators do in fact require an input and an output  
capacitor for stability and smoothing and, therefore, in  
fact only one extra capacitor  $C_1$  would be required. The  
system therefore offers considerable efficiency gains over  
a standard linear regulator through the addition of one  
extra capacitor. The system also offers advantages over  
15       ferro-electric switch mode converters such as buck  
regulators. Capacitors are generally cheaper, smaller,  
have lower series resistance and radiate less than  
inductors and transformers. All of these are qualities  
which are of particular importance for portable  
20       telecommunications systems.

Where higher current applications are required, it is  
necessary to use tantalum or electrolytic capacitors.  
Large transistors are also required for low resistance in  
high current applications.

25       Interference due to high peak charge currents may  
occur, and the switching frequency is not predictable,  
this being dependent on the load current. This can easily  
be overcome by using a fixed frequency clock, rather than  
a comparator to drive the switches. This arrangement,  
30       however, would be less efficient at low loads.

**Claims**

1. A method for controlling a voltage regulator comprising the steps of a) providing first and second charge storage devices switchably connected between a voltage source and the voltage regulator, b) switching the first storage device into connection with the voltage source until the voltage on it reaches a predetermined level, c) disconnecting the first storage device from the voltage source and switching it into connection with the second storage device and the voltage regulator until the voltage input to the voltage regulator falls below a predetermined level, d) repeating steps b) and c).
2. A method according to claim 1 in which the storage devices comprise capacitors connected in parallel with the voltage regulator, across the voltage source.
3. A method according to claim 1 or 2 in which the switching is performed by two switches connected in series, one between the voltage source and the first storage device and the other between the first and second storage devices.
4. A method according to claim 1, 2 or 3 in which the first storage device is significantly larger than the second storage device.
5. Apparatus for controlling a voltage regulator comprising a voltage source, first and second charge storage devices connected between the voltage source and the voltage regulator, means for connecting the first storage device to the voltage source and disconnecting it from the second storage device and the voltage regulator until the voltage on the first storage device reaches a predetermined level, means for disconnecting the first



storage device from the voltage source and connecting it to the second storage device and the voltage regulator until the input voltage to the voltage regulator falls below a predetermined level, means for switching the  
5 storage devices between the 2 modes Of operation.

6. Apparatus according to claim 5 in which the storage devices are capacitors

7. Apparatus according to claim 5 or 6 in which the connecting means comprises two switches are connected in  
10 series between the voltage source and the first storage device, the other between the two storage devices.

8. Apparatus according to claim 4, 6 or 7 in which the first storage device is substantially larger than the second storage device.

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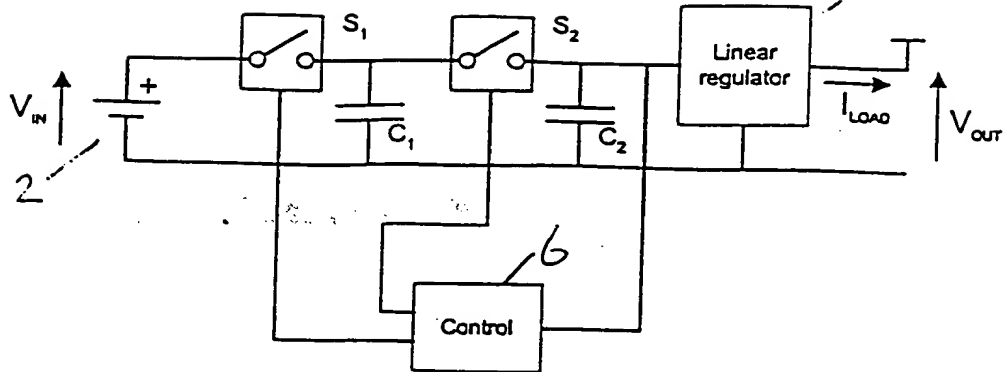


Figure 1

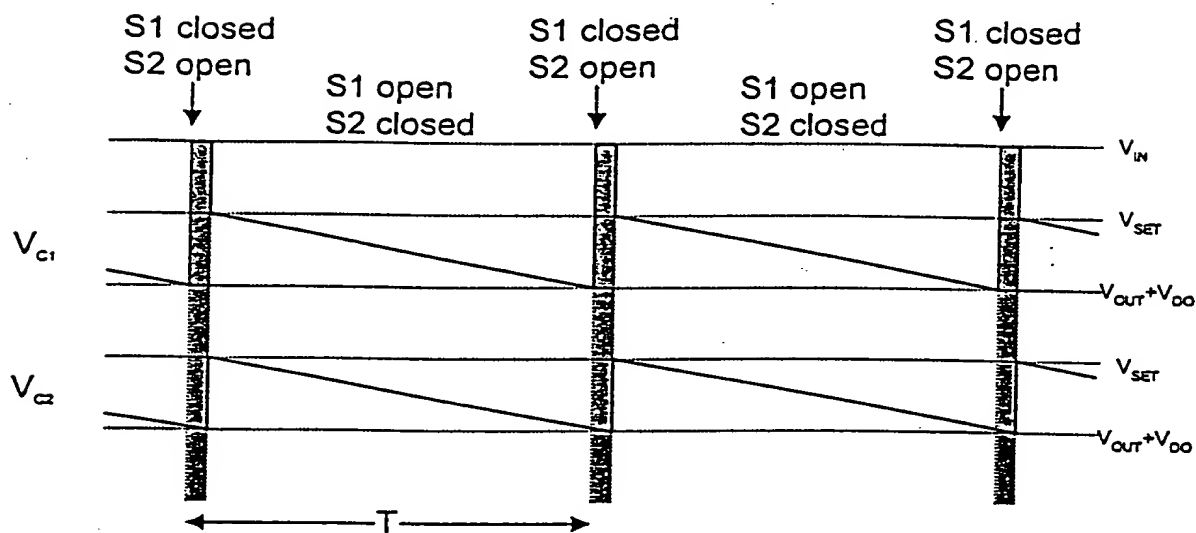


Figure 2

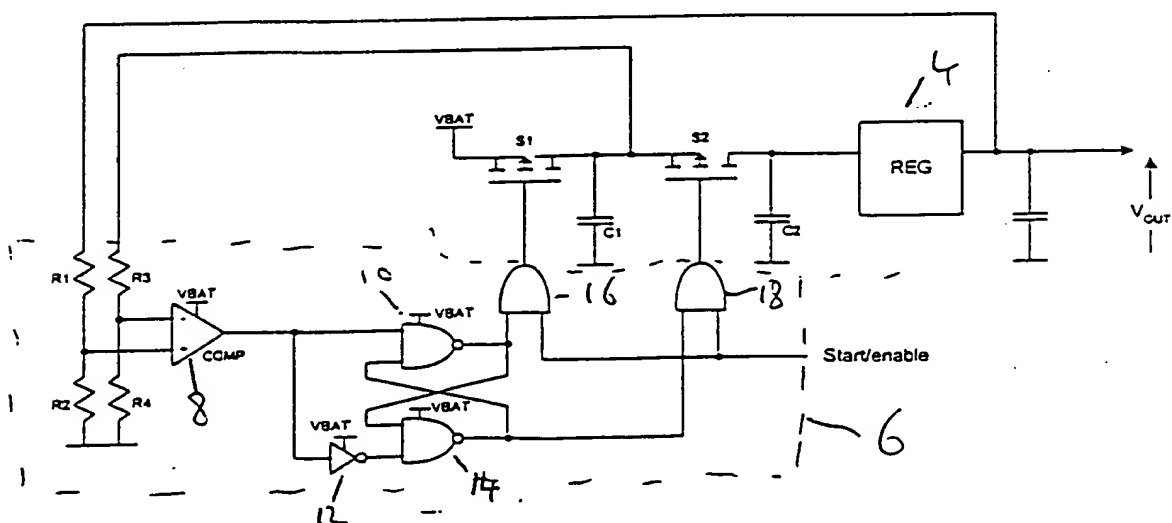


Figure 3

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Start/enable

$V_{comp}$

$I_{V_{comp}}$

$V_{gs1}$

$V_{gs2}$

$V_{C1}$

$V_{C2}$

$I_{in}$

$V_{out}$

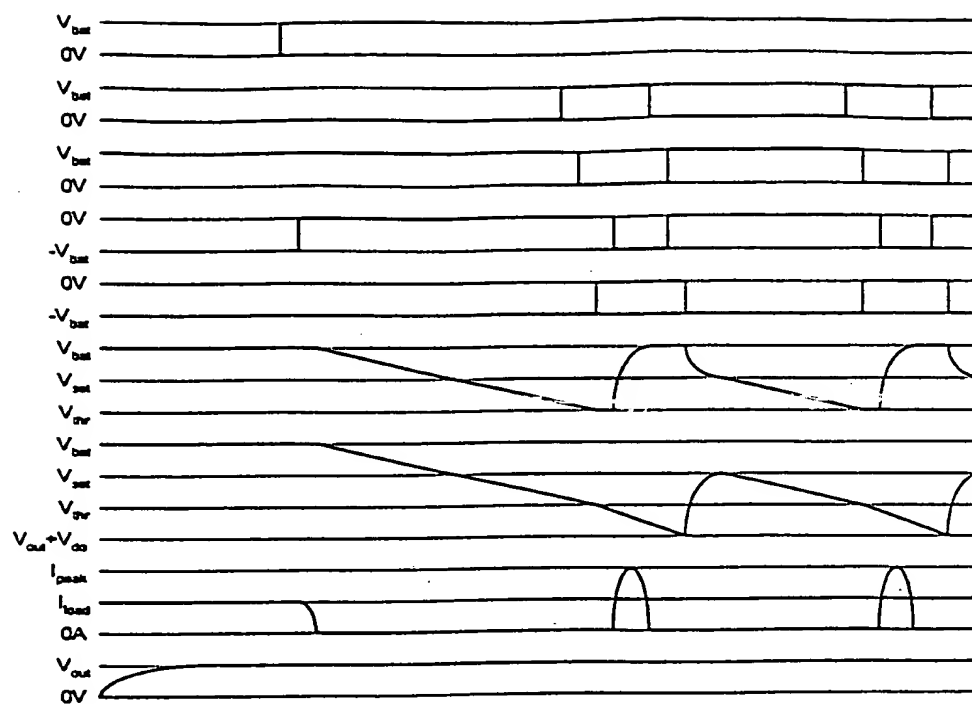


Figure 4

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